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REMARKS

Objections to the claims

Claim 11 has been objected to because the phrase "programmed list of responses" in the last limitation thereof should be "preprogrammed list of responses." Applicant has made this correction.

Claim rejections under 35 USC 102

Claims 1-5, 8-9, and 11-19 have been rejected under 35 USC 102(b) as being anticipated by IBM Technical Disclosure Bulletin, vol. 37, no. 03. Applicant submits that as these claims have been amended, they are no longer anticipated by IBM. There are three claim groups in the claims anticipated by IBM, each beginning with an independent claim: claims 1-5, claims 11-13, claims 14-15, claims 16-17, and claims 18-19. Applicant specifically discusses claim 1 as representative of all of the independent claims; although some of the terminology is different in claim 1 as compared to the other independent claims, for specific purposes of patentability over the prior art cited by the Examiner only, the independent claims can be grouped together. Therefore, in other words, because claim 1 is not anticipated by IBM, neither are the other independent claims, and of course neither are the dependent claims that depend from these independent claims. Applicant provides two independent reasons why the claimed invention is not anticipated by IBM.

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First reason why IBM does not anticipate the claimed invention

Claim 1 as amended is limited to an operation that has "a predetermined responsive output . . . encoded within a transaction lookup table," as well as "an alternative responsive output stored in a register." The Examiner has identified the programmable decode array in FIG. 2 of IBM as the transaction lookup table of the claimed invention. However, the programmable decode array does not store the *predetermined* responsive output in IBM, but rather the *alternative* responsive output – exactly opposite to the claimed invention. As stated on page 324 of IBM:

> [E]very reserved invalid opcode is mapped into a unique address in an array. The array contains an instruction characteristic for each opcode. *To change an opcode from invalid to valid, a new instruction characteristic is written to the array.* Then, whenever this opcode is encountered, it will decode and execute as specified by the characteristic entered in the array.

Indeed, the Examiner admits in the Office Action that the programmable decode array in IBM stores the *alternative* responsive output, and not the predetermined responsive output. As indicated on page 6, paragraph c, of the Office Action, "[t]he multiplexer selects a *substitute* response, *that of the programmable decode array*, in place of the 'normal' response output by a portion of the combinational decode logic."

Thus, both Applicant and the Examiner appear to be in agreement that the programmable decode array of IBM stores the alternative responsive output, not the predetermined responsive output. As such, IBM does not disclose storing the predetermined responsive output in a transaction lookup table, in contradistinction to the claimed invention. Furthermore, insofar as the programmable decode array stores the alternative responsive output in IBM, IBM also does not disclose a register storing the alternative responsive output, as in the claimed invention.

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Second reason why IBM does not anticipate the claimed invention

Claim 1 as amended is further limited to a "comparator comparing the selected identifying information to the operation" such that "a match between the selected identifying information and the operation direct[s] the multiplexer to output the alternative responsive output." The Examiner has identified the combinatorial logic in FIG. 2 of IBM as a comparator, since this logic "takes the opcode as an input and outputs a response dependent on the input." (Office Action, p. 3, para. 7.a.) However, this is not what a comparator is. As presented in the Computer Desktop Encyclopedia definition, filed in the Form 1449 herewith, a comparator is "a device that compares two quantities and determines their equality." Compare this to the Computer Desktop Encyclopedia definition of combinatorial logic, which, as suggested by the Examiner, "refers to a digital logic function . . . in which all outputs of the function are directly related to the current combination of values on its inputs." Combinatorial logic is thus not the same as a comparator, as indicated by the extrinsic evidence.

Combinatorial logic does not compare two quantities to determine their equality, but rather, as indicated by the Examiner, takes an input and provides an output dependent on the input. Indeed, the combinatorial logic in FIG. 2 of IBM could not be a comparator, since it only takes one input and provides two outputs (see FIG. 2 of IBM), whereas a comparator compares two inputs together (see, for instance, FIG. 2 of the patent application as filed). The claimed invention is purposefully limited to a comparator, not combinatorial logic as in IBM. A comparator is a known electronic component, and if IBM had intended to use a comparator, it would have called its component a comparator and not combinatorial logic.

Claim rejections under 35 USC 103

Claims 7 and 10 have been rejected under 35 USC 103(a) as being unpatentable over IBM in view of "The PowerPC Architecture." Claims 7 and 10 are dependent claims, depending from

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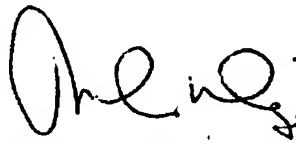Serial no. 10/045,564
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independent claims 1 and 8, respectively, such that they are patentable for at least the reasons that

have been described above.

Conclusion

Applicants have made a diligent effort to place the pending claims in condition for

allowance, and request that they so be allowed. However, should there remain unresolved issues

that require adverse action, it is respectfully requested that the Examiner telephone Applicants'

Attorney so that such issues may be resolved as expeditiously as possible. For these reasons, this

application is now considered to be in condition for allowance and such action is earnestly

solicited.

Respectfully Submitted,

July 11, 2005   _____
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